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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,691	BAILEY, DANIEL WILLIAM	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/1/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: in line 6 the word "its" is recited. It's unclear therefore applicant is suggested to replace "its" by the proper meaning. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-15 and 17-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Elliot et al U.S. Patent No 6,826,247 B1.

As per claims 1 and 19 Elliot et al teaches a locked loop system that synchronizes a clocked signal to a reference clock signal, comprising: a phase detector (see figs.2, 5 and 4 elements 224, 505 and col.4, lines 41-67 and col.5, lines 42-67 and col.8, lines 52-67 and col.9, lines 1-6) that detects a difference in phase between the clocked signal and the reference clock signal, and generates an output signal indicating the phase difference; a digital counter (see fig.2, 5 elements 208, 514 or 516 or 518 and col.9, lines 42-45 and col.10, lines 17-67) coupled to the phase detector, said digital counter receiving the output signal generated by the phase detector, and in response,

modifying its count value and generating a binary output signal indicating said count value; an electronic circuit coupled to said digital counter, said electronic circuit being configured to receive said binary output signal, and in response, generate a thermometer-coded (see col.7,lines 46-67 and col.8, lines 4-5 and see fig.5 element 506 and col.9, lines 24-28) output signal that corresponds to said binary output signal; and a delay line coupled to said electronic circuit, said delay line including a plurality of delay elements (see figs.2, 5 elements 202, 507 and col.5, lines 2-20 and col.8, lines 40-63) that are enabled by said thermometer-coded output signal.

As per claim 2, Elliot et al does teach wherein the digital locked loop system comprises a digital delay locked loop (see col.5, lines 1, 16-18).

As per claim 3, Elliot et al does teach, wherein the digital locked loop system comprises a digital phase locked loop (see fig.1 element 108 and col.6, line 36).

As per claim 4, Elliot et al does teach, wherein the clocked signal comprises a feedback clock generated by said delay line, and the reference clock signal comprises a synchronized clock signal (see fig.2).

As per claim 5, Elliot et does teach wherein the output signal generated by the phase detector includes an increment count signal and a decrement clock signal, depending on if the clocked signal lags or leads the reference clock signal (see col.9, lines 40-45 and col.10, lines 17-20).

As per claim 6, Elliot et al does teach wherein the digital counter increases its count value in response to the increment count signal, and decreases its count value in response to the decrement clock signal (see col.9, lines 40-45).

As per claim 7, Elliot et al inherently teach wherein the thermometer-coded output signal includes m output signals, and the binary output signal generated by the digital counter includes x output signals, and wherein the m output signals approximately equals 2.sup.x.

As per claim 8, Elliot et al does teach wherein the electronic circuit comprises comparator logic (see col.9, lines 50-62).

As per claim 9, Elliot et al inherently teaches, wherein the comparator logic includes a first comparator and a second comparator.

As per claim 10, Elliot et al inherently teach wherein the first comparator receive said binary output signal from said digital counter, and in response generates threshold values.

As per claim 11, Elliot et al inherently teach wherein the second comparator receives said threshold values, and generates said a thermometer-coded output signals.

As per claim 12, Elliot et al does teaches comprises a plurality of logical units (see col.3, lines 26-7) that generate said thermometer-coded output signal on a plurality of output signal lines. Furthermore implement such teaching into the second comparator is inherently taught by Elliot et al.

As per claim 13, Elliot et al inherently teaches wherein the binary output signals are transmitted from said digital counter on a plurality of output lines, and wherein the number of output signal lines of said second comparator exceed the number of output lines of said digital counter.

As per claim 14, Elliot et al does teaches, wherein each of said plurality of logical units has an associated output signal line, and wherein each logical unit generates an enable signal that is transmitted on the associated output signal line.

As per claim 15, Elliot et al does teaches, wherein each of said plurality of logical units receives at least one of said threshold values from said first comparator, and in response generates a pair of enable signals.

As per claim 17, Elliot et al inherently teaches, wherein each logical unit includes a high pass gate that generates one of said pair of enable signals, and a low pass gate which generates the other of said pair of enable signals.

As per claim 18, Elliot et al does teach wherein said logical unit further includes combinatorial logic (see col.3, lines 26-7). Furthermore implement such teaching to combine together threshold values from said first comparator is inherently taught by Elliot et al.

As per claim 20, Elliot et al does teach wherein the delay line comprises a plurality of delay elements (see figs.2, 5 elements 202, 502 and col.5, lines 13-20 and col.8, lines 53-67), and wherein each of said second plurality of output signal lines enables one of said plurality of delay elements.

As per claim 21, Elliot et al inherently teaches wherein the second plurality of output signal lines is greater in number than the first plurality of signal lines.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 16, 22-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elliot et al U.S. Patent No 6,826,247 B1 in view of Landman et al U.S. patent No 6,028,488.

As per claims 16 and 22, Elliot et al teaches all the features of the claimed invention except wherein said plurality of delay elements each comprise a transistor stack, and wherein each transistor stack is enabled by the enable signal from an associated output signal line of said second comparator.

Landman teaches said plurality of delay elements each comprises a transistor stack, and wherein each transistor stack (see fig.1c and col.4, lines 15-30 and col.10, lines 10-201). Furthermore implementing such teaching to enable signal from associated output line of a second comparator would have been obvious to one skilled in the art as to accurately recover the phase clock in the incoming signal.

As per claim 23 Elliot and Landman in combination would teach wherein the act of converting includes establishing a plurality of threshold values corresponding to said binary count value signal as to accurately recover the phase clock in the incoming signal at any time interval during the synchronization process.

As per claim 24 Elliot and Landman in combination would teach wherein the plurality of threshold values are selectively combined to generate the thermometer-coded signal on said second plurality of output signal lines as to accurately recover the phase clock in the incoming signal at any time interval during the synchronization process.

As per claim 25, Elliot teaches a digital delay locked loop that controls the amount of delay to apply to a clocked signal to synchronize with a reference signal, comprising: a phase detector that determines (see figs.2, 5 and 4 elements 224, 505 and col.4, lines 41-67 and col.5, lines 42-67 and col.8, lines 52-67 and col.9, lines 1-6) a difference in phase between the clocked signal and the reference signal, and which generates an output signal that indicates if the clocked signal is ahead of or behind the reference signal; a binary counter (see fig.2, 5 elements 208, 514 or 516 or 518 and col.9, lines 42-45 and col.10, lines 17-67) that produces a binary output signal that indicates a desired delay for said clocked signal based on a count value produced in response to said output signal from said phase detector; comparator logic (see col.9, lines 50-62) that establishes threshold values for said binary output signal, and which generates a plurality of enable output signal based on said threshold values; and a delay (see figs.2, 5 elements 202, 507 and col.5, lines 2-20 and col.8, lines 40-63) line 26. A system as in claim 25, wherein the clocked signal produced by said delay line is applied to an input of the phase detector as the clocked signal.

However Elliot does not teach a delay that includes a plurality of transistor stacks arranged in parallel, and wherein each of said plurality of said enable signals

controls one of said plurality of transistor stacks to thereby control the amount of delay given to said clocked signal.

Landman teaches a delay that includes a plurality of transistor stacks arranged in parallel, and wherein each of said plurality of said enable signals controls one of said plurality of transistor stacks to thereby control the amount of delay given to said clocked signal (see fig.1c and col.4, lines 15-30 and col.10, lines 10-201).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Landman into Elliot as to accurately recover the phase clock in the incoming signal at any time interval during the synchronization process.

As per claim 27, Elliot and Landman would teach wherein the plurality of enable output signals are provided on a plurality of output signal lines between the comparator logic and the delay line as to accurately recover the phase clock in the incoming signal at any time interval during the synchronization process.

As per claim 28, Elliot teaches, wherein the plurality of enable output signals are encoded on said plurality of output signal lines as a thermometer-coded signal (see col.7, lines 50-67).

As per claim 29, Elliot teaches, wherein the output signal generated by the phase detector includes an increment count signal and a decrement clock signal, depending on if the clocked signal lags or leads the reference clock signal (see col.9, lines 40-45 and col.10, lines 17-20).

As per claim 30, Elliot teaches wherein the binary counter increases the count value in response to the increment count signal, and decreases its count value in

response to the decrement clock signal (see col.9, lines 40-45 and col.10, lines 17-20).

As per claim 31, Elliot teaches, wherein the comparator logic comprises a plurality of logical units that generate said thermometer-coded output signal on a plurality of output signal lines.

As per claim 32 Elliot teaches wherein each of said plurality of logical units (see col.3, lines 26-7) has an associated output signal line, and wherein each logical unit generates an enable signal that is transmitted on the associated output signal line.

As per claim 33, Elliot and Landman would teach wherein each of said plurality of logical units receives at least one threshold value, and in response generates a pair of enable signals as to accurately recover the phase clock in the incoming signal at any time interval during the synchronization process.

As per claim 34, Elliot and Landman would teach, wherein each logical unit includes a high pass gate that generates one of said pair of enable signals, and a low pass gate which generates the other of said pair of enable signals as to accurately recover the phase clock in the incoming signal at any time interval during the synchronization process.

As per claim 35, Elliot teaches wherein said logical unit further includes combinatorial logic (see col.3, lines 26-7). Furthermore implement such teaching into Landman for combining together some of said threshold values would have been obvious to one skilled in the art as to accurately recover the phase clock in the incoming signal at any time interval during the synchronization process.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Xanthopoulos U.S. Pub No 2002/0079937 A1 teaches a digital phase locked loop (***).

Bhullar et al U.S. patent No 6,683,928 B2 teaches a process voltage temperature (***).

Kotra U.S. patent No 6,518,809 B1 teaches a clock circuit.

Lutkemeyer U.S. patent No 6,693,475 B2 teaches a system and method for compensating.

Gomm et al U.S. patent No 6,803,826 B2 teaches a delay locked loop circuit (***).

Saeki U.S. patent No 6,380,774 B2 teaches a clock control circuit.

Staszewski et al U.S. patent No 2002/0033737 A1 teaches a system and method for time dithering.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2631

1/28/05

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